

Low-Resistance Ohmic Contacts for Microwave and Lightwave Devices

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Abstract—High-speed solid-state devices for use in microwave and lightwave circuits require high quality ohmic contacts to *n*- or *p*-type compound semiconductor layers. The fabrication and electrical properties of a multilayer ohmic contact with contact resistances in the 10^{-7} ohm-cm² range on both *n*- and *p*-type materials are reported.

LOW-RESISTANCE ohmic contacts have wide importance for the fabrication of microwave and photonic devices. The need for higher speed devices with smaller and more complex geometries has placed greater demands on the performance of ohmic contacts. A good contact should have a linear I-V characteristic, be stable over time and temperature, and contribute as little parasitic resistance to the devices as possible ([1]–[6]).

We report on the fabrication of low-resistance ohmic contacts to *n*- and *p*-type compound semiconductor layers. Each contact consists of a five layer structure of evaporated metal that is alloyed at a critical temperature. Measurements of the alloyed contacts gave resistances in the 10^{-7} ohm-cm² range, which is lower than previously obtained results from conventional three layer metallization systems produced by evaporation of an appropriate eutectic alloy. For example, our previous *p*⁺ type contacts on InP substrates for lightwave devices were made by evaporation of an AuZn alloy (5% by weight Zn) and resulted in contacts with a resistance of 6×10^{-6} ohm-cm². In addition these resistance values were difficult to reproduce because of the rapid depletion of Zn caused by fractional distillation from the evaporation source. It should also be pointed out, that information on these type of contacts is sparse and difficult to obtain. The morphology of the contacts was excellent with good linewidth control and completely reproducible results, which makes them useful for fabricating high-speed devices with low series resistances and high cut-off frequencies.

Metal-semiconductor ohmic contacts were formed on thin *n*-type gallium arsenide ($2 \times 10^{18}/\text{cm}^3$) and *p*-type indium phosphide ($2 \times 10^{18}/\text{cm}^3$) epitaxially grown layers on semi-insulating substrates. Photo-optically generated patterns were outlined on the surface of the substrate with a standard lithography process. In addition, a chlorobenzene soak was used to form a lip on the edge of the photoresist pattern. The importance is twofold, it makes the development time less critical in terms of obtained feature size and enables one to get sharp edges for lift-off after the metallization is deposited.

The ohmic contact metallization is deposited over the entire surface using an electron beam evaporator. A cross-sectional view of the layers required for fabricating *n*-type and *p*-type contacts is shown in Fig. 1. For an *n*-type contact they consist

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FIVE-LAYER OHMIC CONTACT STRUCTURE

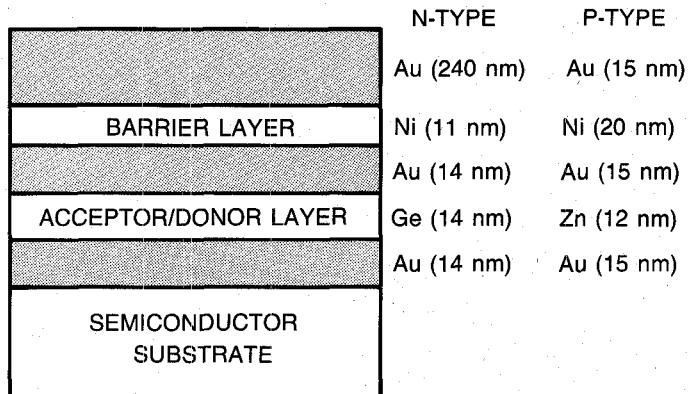


Fig. 1. Cross-sectional view of evaporated metal layers on semiconductor substrate. Germanium is used as a donor layer for *n*-type contacts on GaAs, and a film of zinc provides the acceptors for *p*-type contacts on InP.

of a bottom layer of gold (14 nm), followed by a donor layer of germanium (14 nm), a middle layer of gold (14 nm), a barrier layer of nickel (11 nm), and a top layer of gold (240 nm). Similarly, the *p*-type contact consists of a layer of gold (15 nm), followed by an acceptor layer of zinc (12 nm), a middle layer of gold (15 nm), a barrier layer of nickel (20 nm) and a top layer of gold (150 nm). This five-layer ohmic contact structure has the following advantages compared to conventional approaches.

- The donor/acceptor layer is clearly separated from the barrier layer. This prevents undesired chemical reactions between the dopants and the barrier.
- Evaporation of eutectic alloys containing the dopants is not necessary. Thus fractional distillation in the evaporation process is avoided and the resulting contacts show better reproducibility.
- The top gold layer is sufficiently thick to permit bonding. A post evaporation of gold over the alloyed area is not needed.
- Only three metal evaporation sources are required to create the five-layer structure.

After depositing the layers the photoresist and metal stencil are removed by soaking in organic solvents to leave a clean, sharp pattern.

Alloying of the deposited layers to form the ohmic contact is performed on a strip heater, which consists of a carbon block on top of a tantalum foil that is uniformly heated and monitored with a thermocouple in a forming gas atmosphere. The temperature cycle to alloy the metal layers to the semiconductor surface for the *n*-type contact includes a temperature rise to 425°C in 60 seconds, followed by a thermal soak for an additional 60 seconds and then rapid cooling to < 50°C in 15 seconds. A maximum

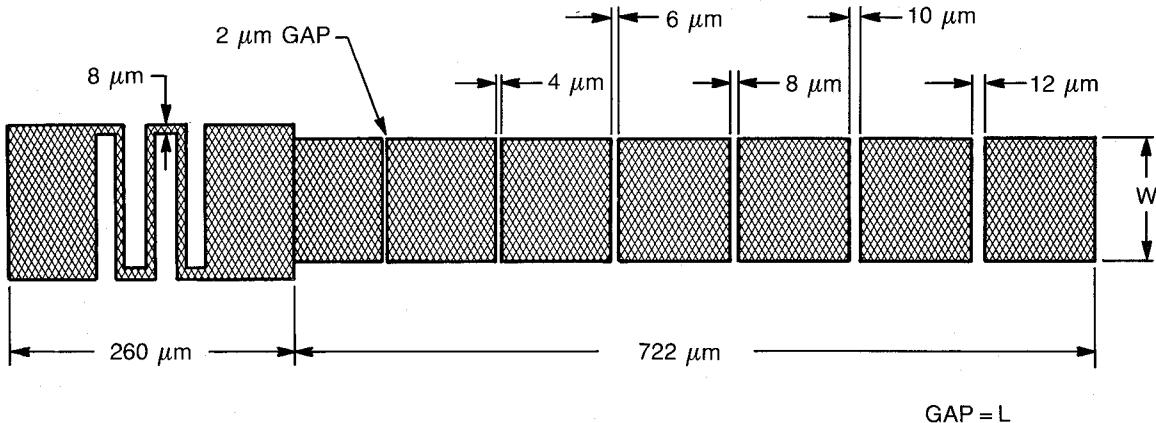


Fig. 2. Test pattern used to determine the specific contact resistance of the deposited metalization through use of the transfer length method. The pattern consists of contact pads formed on the surface of the semiconductor that are separated by a distance L . Contacts have a width W and are separated by gaps ranging from 2 μm to 12 μm .

alloying temperature of 475°C is used for the p -type contact. After completing the alloying process the surface remains smooth for both metallization schemes.

The resistance associated with a planar ohmic contact is defined to be the resistance between the metal and an imaginary plane that is at the edge of and perpendicular to the metalization. It has a two part contribution, made up of the characteristics of the conducting layer on which it is formed, and the specific contact resistance of the metalization deposited. This latter contribution is the focus of this letter.

The specific contact resistance of the deposited metalization can be determined through use of the transfer length method that requires fabrication of a suitable test pattern on the semiconductor surface. This test structure, shown in Fig. 2, typically consists of an array of differently spaced contact pads formed on the surface of the semiconductor which are separated by a distance L . The contacts have a width W and are isolated to restrict current flow only across the distance L .

The resistance between each contact pad is measured with a set of four probes, two of which supply a constant current and the other two for measurement of the voltage. This measured resistance is the gap resistance R , which when plotted versus the pad spacing L , gives a straight line. It consists of the contribution of the two contact pads plus the resistance of the semiconductor layer between them.

The specific contact resistance r_c of the alloyed film can then be calculated from

$$r_c = \frac{1}{2} R_c W L_x. \quad (1)$$

The parameters of this equation can easily be evaluated from the graphical data obtained from plots shown in Fig. 3. The results obtained for the contact resistance are given in the table shown in Fig. 3. The p -type contact displays a gap resistance that is slightly higher than that for the n -type contact. The resulting specific contact resistance is $8.8 \times 10^{-7} \text{ ohm-cm}^2$ for n -type contacts and $9.5 \times 10^{-7} \text{ ohm-cm}^2$ for p -type contacts. A total of 40 measurements were made for the n^+ contact, spreading over a range of $\pm 20\%$. For the p^+ contact the lowest value was $7 \times 10^{-7} \text{ ohm-cm}^2$ and the highest value was $1.2 \times 10^{-6} \text{ ohm-cm}^2$. Although no other compound semiconductor structures were investigated it is our belief that this five-layer struc-

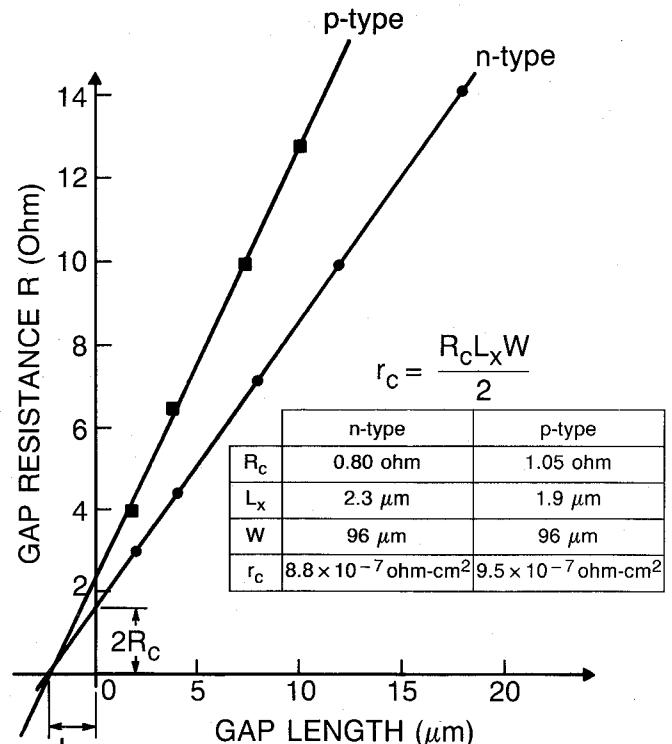


Fig. 3. Transfer length measurement showing plot of the measured gap resistance versus the contact pad spacing. Specific contact resistance r_c of the deposited metalization is calculated from the x - and y -intercepts.

ture looks attractive for a wide range of other semiconductor possibilities. The metalization technique described in this letter are applicable for fabricating a wide variety of microwave and lightwave devices including switching diodes, field effect transistors, buried heterostructure DFB lasers, and InP based quantum well lasers described recently by Temkin, *et al.* [7].

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